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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,423	08/01/2003	Shawn G. Quick	100204386-1	4366

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EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,423	QUICK, SHAWN G.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☒ Claim(s) *27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The Oath filed June 6, 2003 complies with all the requirements set fort in MPEP 602 and therefore is accepted.

Drawings

The filed drawings are accepted.

Specification

The disclosure is objected to because of the following informalities:

The abstract of the disclosure is objected to because it does not describe the disclosure sufficiently. The applicant needs to describe the invention in more detail. Correction is required. See MPEP § 608.01(b).

Applicant inappropriately uses "Thusly" (page 5, line 10 & page 6, line 8) it should be thus. Appropriate correction is required.

Claim Objections

Claims 27 & 28 are objected to because of the following informalities:

As per claim 27:

This claims links its dependency to itself. For the purpose of compact prosecution it is presumed that the applicant intended to link the dependency to claim 26 rather than claim 27. Applicant should change "27" to "26."

As per claim 28:

This claim is objected to by virtue of their dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-24, 26, 27, & 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Hofstee et al. US Pat no. 6,751,749 B2.

As per claim 1:

Hofstee et al. teaches a method for testing code comprising: instrumenting code to output checkpoints at selected points during execution of said code on a processor device to derive individual test checkpoints (columns 2-3, lines 64-3); and generating a signature using said checkpoints (Figure 5 # 444A & 444B, column 2, lines 47-48).

As per claim 2:

Hofstee et al. teaches the method of claim 1 wherein said checkpoints comprising said signature are arranged in an order of execution of functions associated with said checkpoints (column 2, lines 48-54).

As per claim 3:

Hofstee et al. teaches the method of claim 2 further comprising comparing said signature against an expected signature for said code (Figure 5 # 420, column 6, lines 33-42)

As per claim 4:

Hofstee et al. teaches the method of claim 4 wherein said comparing comprises comparing order of execution of said functions of said code (Figure 4 # 440A, column 4, lines 45-46).

As per claim 5:

Hofstee et al. teaches the method of claim 4 wherein said comparing is carried out offline (Figure 5 # 420, it can be seen that the compare unit is a separate entity, hence operating offline).

As per claim 6:

Hofstee et al. teaches the method of claim 1 further comprising repeating said execution of the instrumented code and said generating on a second processor device, commonly configured to first said processor device (Figure 5, # 410B, column 6, lines 61-65).

As per claim 7:

Hofstee et al. teaches the method of claim 6 further comprising comparing signatures, from execution of said code on each of said processor devices, against each other (Figure 5 # 420, column 4, lines 50-63).

As per claim 8:

Hofstee et al. teaches the method of claim 1 further comprising: instrumenting a successive version of said code for execution on said processor device to derive a successive stream of test checkpoints (column 3, lines 15-16); generating a successive

signature using said successive checkpoints (columns 5-6, lines 66-2); and comparing said successive signature against first said signature (column 6, lines 40-43).

As per claim 9:

Hofstee et al. teaches the method of claim 8 wherein said checkpoints comprising said first said signature and said successive signature are arranged in an order of functions associated with said checkpoints (column 6, line 9-18).

As per claim 10:

Hofstee et al. teaches the method of claim 1 further comprising: instrumenting a successive version of said code for execution on a second processor device (column 6, lines 26-27), commonly configured with first said processor device (Figure 5, instructions 510), to derive a second stream of test checkpoints (column 6, lines 26-27); generating a successive signature using said successive checkpoints (Figure 5, # 520 A & 520 B, column 6, lines 5-9); and comparing said successive signature against said signature (column 6, line 40-43).

As per claim 11:

Hofstee et al. teaches the method of claim 10 wherein said checkpoints comprising said first signature and said successive signature are arranged in an order of execution of said functions associated with said checkpoints (Figure 5, instructions 510, column 6, lines 9-14).

As per claim 12:

Hofstee et al. teaches the method of claim 1 further comprising: comparing said signature against an archived signature for said code (column 2, lines 39-46).

As per claim 13:

Hofstee et al. teaches the method of claim 12 further comprising: detecting, by said comparing step, modifications to said code (column 6, lines 42-43).

As per claim 14:

Hofstee et al. teaches the method of claim 12 further comprising: debugging said code based on differences in said signature and said archived signature (column 6, lines 44-50).

As per claim 15:

Hofstee et al. teaches the method of claim 1 further comprising: identifying said code from said signature (column 6, lines 1-10).

As per claim 16:

Hofstee et al. teaches the method of claim 1 further comprising: identifying a function of said code from a portion of said signature (column 6, lines 28-33).

As per claim 17:

Hofstee et al. teaches the method of claim 16 further comprising: mapping a function of said code by placement of at least one of said checkpoints in conjunction with said function (column 6, lines 34-39).

As per claim 18:

Hofstee et al. teaches the method of claim 17 wherein said instrumenting further comprises placing one checkpoint before said function and another checkpoint after said function (column 6, lines 9-16).

As per claim 19:

Hofstee et al. teaches the method of claim 17 further comprising: determining code functions executed by said processing device by identifying output of checkpoints placed in conjunction with said functions (Figure 7 # 715, column 8, lines 20-25).

As per claim 20:

Hofstee et al. teaches the method of claim 19 further comprising: deriving execution paths of said code from said signature through order of execution of said functions (column 8, lines 26-34).

As per claim 21:

Hofstee et al. teaches the method of claim 17 further comprising: detecting an error in execution of said code by identifying output checkpoints placed in conjunction with an error path function of said code (Figure 7 # 760, columns 8-7, lines 63-4).

As per claim 22:

Hofstee et al. teaches the method of claim 1 further comprising: archiving said signature (column 2, lines 39-44); merging said instrumented code to a second processor platform (column 2, lines 47-54); executing said instrumented code on said second processor platform to derive a second stream of individual test checkpoints (column 2, lines 33-36); generating a second signature using said second stream of checkpoints (column 2, lines 32-34) and comparing said second signature against said archived signature (column 2, lines 54-56).

As per claim 23:

Hofstee et al. teaches the method of claim 22 wherein said checkpoints comprising said archived signature and said second signature are arranged in an order of execution of said tests (column 4, lines 53-59).

As per claim 24:

Hofstee et al. teaches the method of claim 1 wherein said processor device is a computer (Figure 4 # 400).

As per claim 26:

Hofstee et al. teaches a system for testing code comprising: an under test processor based device executing said code (Figure 5, # 410A & 410B), wherein said code is instrumented to output checkpoints at selected points during execution (columns 2-3, lines 64-3), said processor device adapted to output said checkpoints in a stream (column 6, lines 26-27); and an external processor device receiving said output checkpoint stream and deriving a checkpoint signature for execution of said code from said stream (Figure 5 # 444A & 444B, column 2, lines 47-48).

As per claim 27:

Hofstee et al. teaches the system of claim 26 wherein firmware of said under test processor based system provides said code (Figure 5, Instructions 510).

As per claim 29:

Hofstee et al. teaches a method for merging code from a source processor platform to a target processor platform (column 6, lines 28-35) said method comprising: implementing said code to output checkpoints at selected points during execution of said code on a target processor platform to derive a stream of individual test

checkpoints (column 6, lines 26-27); generating an ordered signature using said checkpoints (columns 5-6, lines 66-2); and comparing said signature against an archived signature derived from successful execution of said code on a source processor platform (column 2, lines 39-46).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 25 & 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofstee et al. US Pat no. 6,751,749 B2.

As per claim 25:

Hofstee et al. substantially teaches a method for testing code comprising: instrumenting code to output checkpoints at selected points during execution of said

code on a processor device to derive individual test checkpoints (columns 2-3, lines 64-3); and generating a signature using said checkpoints (Figure 5 # 444A & 444B, column 2, lines 47-48).

Hofstee et al. does not explicitly teach the method wherein said processor device is a simulator.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a simulator as the said processor device (column 9, lines 34-36), since it was known in the art that it is best to perform the functions on a simulator to assist in an efficient construction and predictable functioning of the actual hardware. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized to use a simulator, as the said processor device would have allowed for an efficient construction and predictable functioning of the actual hardware.

As per claim 28:

Hofstee et al. substantially teaches a system for testing code comprising: an under test processor based device executing said code (Figure 5, # 410A & 410B), wherein said code is instrumented to output checkpoints at selected points during execution (columns 2-3, lines 64-3), said processor device adapted to output said checkpoints in a stream (column 6, lines 26-27); an external processor device receiving said output checkpoint stream and deriving a checkpoint signature for execution of said code from said stream (Figure 5 # 444A & 444B, column 2, lines 47-48), wherein

firmware of said under test processor based system provides said code (Figure 5, Instructions 510).

Hofstee et al. does not explicitly teach the method wherein said under test processor based device executes said code as part of a simulation of another processor based device.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the method wherein said under test processor based device executes said code as part of a simulation of another processor based device (column 9, lines 34-36), since it was known in the art that it is best to perform the functions on a simulator to assist in an efficient construction and predictable functioning of the actual hardware. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized to use a simulator, as the said processor device would have allowed for an efficient construction and predictable functioning of the actual hardware.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US Pat no. 3,983,535 A, US Pat no. 6,513,050 B1, US Pat no. 6,571,363 B1, US Pat no. 6,718,538 B1, US Pat no. 6,874,138 B1, and Non Patent Literature Research Disclosure 427067 mention the same pattern of processing system having multiple processors, using checkpoints to generate signatures are included herein for Applicant's review.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

Saqib Siddiqui
Art Unit 2138
12/16/2005

GUY LAMARRE
PRIMARY EXAMINER